Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

FEATURES

Synchronization and horizontal part

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Triple current source in the phase detector with automatic selection
- Normal phase detector time constant is increased to fast during the vertical blanking period (external switching for VTR conditions not necessary)
- Slow phase detector time constant and gated sync pulse operation are automatically switched on by an internal sync pulse noise level detection circuit
- Fast phase detector time is switched on for locking
- Time constant externally switchable
- Inhibit of horizontal phase detector and video transmitter identification circuit during equalizing pulses and vertical sync pulse
- Inhibit of horizontal phase detector during separated vertical sync pulse
- Second phase detector for storage compensation of the line output stage
- 3-level sandcastle pulse generator
- Automatic adaption of the burst key pulse width
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Horizontal output current with constant duty factor value of 55%
- Duty factor of the horizontal output pulse is 55% when the horizontal flyback pulse is absent.

Vertical part

- f_V = 60 Hz (M) system
- Vertical synchronization pulse separator without external components and two integration times
- Zener diode reference voltage source for the vertical sawtooth generator and vertical comparator
- Divider system with three different reset enable windows
- Synchronization is set to 528 divider ratio when no vertical sync pulse and no video transmitter is identified
- Divider window is forced to wide window when a vertical sync pulse is detected within the window provided by reset divider and end of vertical blanking period, on condition that the voltage on pin 18 is ≤1.2 V
- Divider ratio is 528 (f_V = 60 Hz) for DC signal on pin 5
- Linear negative-going sawtooth generated via the divider system (no frequency adjustment)
- Comparator with low DC level feedback signal
- Output stage driver
- f_V = 60 Hz identification output combined with mute function
- Start of vertical blanking is shifted to the start of the pre-equalizing pulses when the divider ratio is between 522 and 528 lines per picture
- Guard circuit which generates the vertical blanking pulse level on the sandcastle output pin 17 when the feedback level at pin 2 is not within the specified limits.

GENERAL DESCRIPTION

The TDA2579C is an integrated circuit generating all requirements for synchronization of its horizontal oscillator and output stage plus those of the vertical part which comprises a divider system, sawtooth generator, comparator and output stage.
The TDA2579C is almost identical to the TDA2579B.
It is optimized for the M (60 Hz) TV system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2579C	18	DIL	plastic	SOT102

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{16}	minimum required current for starting horizontal oscillator and output stage		6.2	–	–	mA
V_{10}	main supply voltage		–	12	–	V
I_{10}	supply current		–	70	–	mA
Input signals						
V_{5-9}	sync pulse input amplitude		0.05	–	1	V
I_{12}	horizontal flyback pulse input current		0.2	1	–	mA
V_2	vertical comparator input voltage					
	AC (peak-to-peak value)		–	0.8	–	V
	DC		–	1	–	V
Output signals						
V_{11}	horizontal output voltage (open collector)	I_{11} = 25 mA	–	–	0.5	V
V_1	vertical output stage driver (emitter follower)	I_1 = 1.5 mA	5	–	–	V
V_{17}	sandcastle output voltage levels					
	burst key		9.8	–	–	V
	horizontal blanking		–	4.5	–	V
	vertical blanking		–	2.5	–	V
VIDEO TRANSMITTER IDENTIFICATION OUTPUT; note 1						
V_{13}	output voltage	no sync pulse present	–	–	0.32	V
I_{13}	output current	no sync pulse present	–	–	5	mA
V_{13}	output voltage	sync pulse present; divider ratio <576	–	7.6	–	V

Note

1. Open collector loaded with external resistor to positive supply.

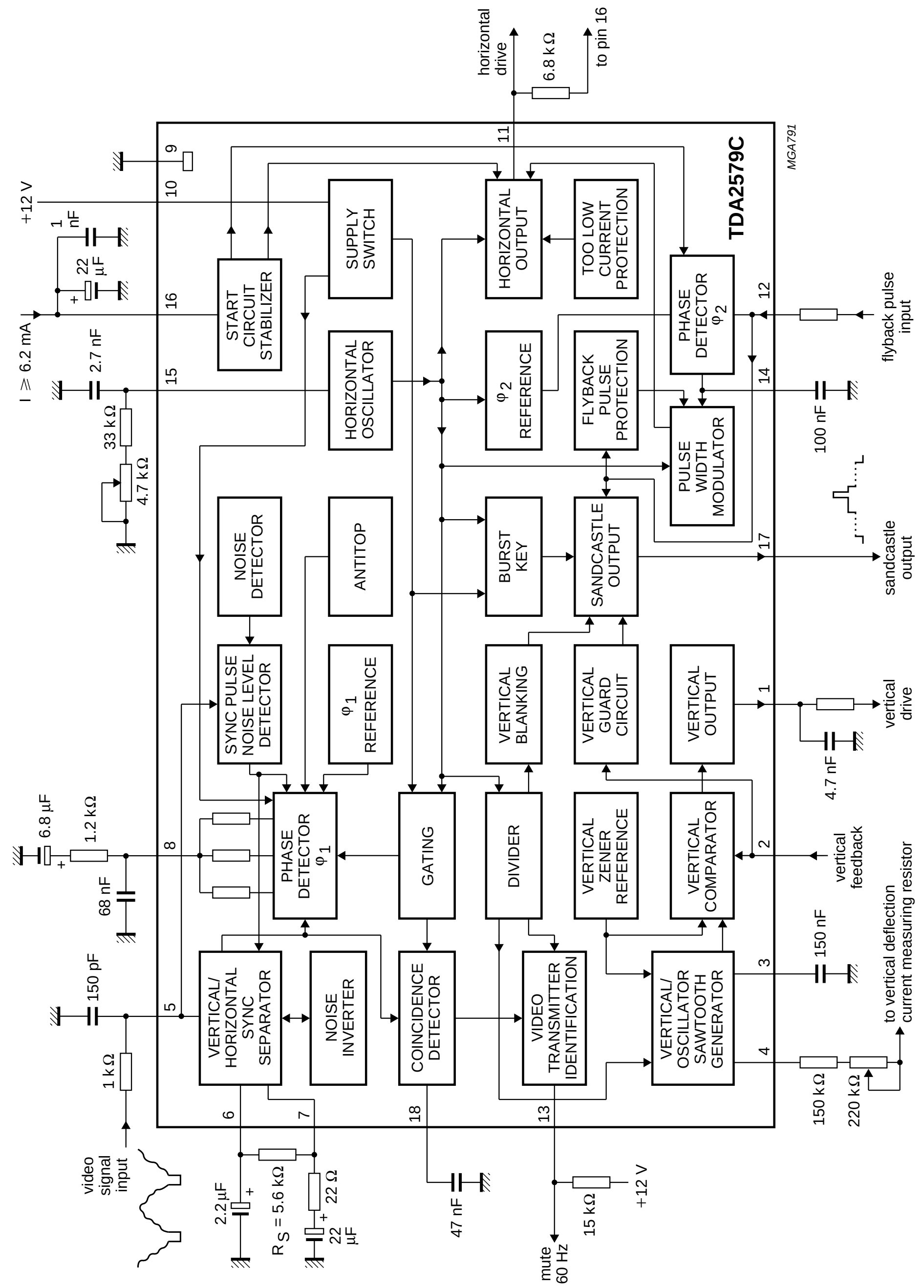


Fig.1 Block diagram.

Synchronization circuit with synchronized vertical divider system for 60 Hz

TDA2579C

PINNING

SYMBOL	PIN	DESCRIPTION
V_{OUT}	1	vertical driver output
FB	2	vertical feedback input
SAW	3	vertical sawtooth generator
VDC	4	vertical deflection current output
VID	5	video signal input
CSL	6	slicing level storage capacitor
RSL	7	slicing level resistor
φ_1	8	phase detector φ_1
GND	9	ground (0 V)
V_P	10	main supply voltage (+12 V)
H_{OUT}	11	horizontal driver output
FLYB	12	horizontal flyback pulse input
MUTE	13	mute output
H_{SHIFT}	14	horizontal picture shift capacitor
H_{OSC}	15	horizontal oscillator frequency setting
STAB	16	start circuit stabilizer input
SC	17	sandcastle output
DET	18	coincidence detector output

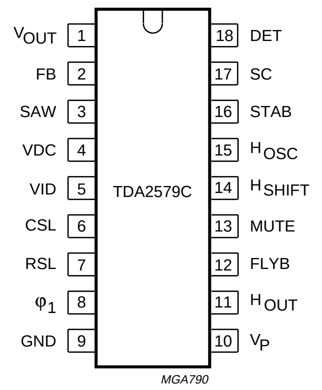


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2579C generates both horizontal and vertical drive signals, a 3-level sandcastle output pulse, a transmitter identification signal and 60 Hz window information.

The horizontal oscillator and horizontal output stage functions are started via the supply current into pin 16. The required current has a typical value of 5 mA which can be taken directly from the mains rectifier. The horizontal output transistor at pin 11 is not conducting until the supply current at pin 16 has reached its typical value. The starting circuit has a hysteresis of approximately 1 mA. The horizontal output current of pin 11 starts at a duty cycle of 60%. All other IC functions are enabled via the main supply voltage on pin 10.

The pin 16 supply system enables slaved synchronized switch mode systems in which the horizontal output signal of the TDA2579C is used as master signal. In such a system the 12 V supply (main supply at pin 10) can be generated by the line output stage.

An internal Zener diode reference voltage is used for the vertical processing part. The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. Thus no vertical frequency adjustment is required.

The circuit operation is restricted to the M (f_V = 60 Hz) system.

Vertical part (pins 1, 2, 3 and 4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, thus the horizontal oscillator is operating at its nominal line frequency and one line period equals 2 clock pulses. No vertical frequency adjustment is required due to the divider system. The divider system operates with 3 different reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its value by 1 each time the separated vertical sync pulse is within the window being searched. The count is reduced by 1 when the vertical sync pulse is not present.

The reset of the counter system (clock pulse 0) is at half a line period after the start of the vertical pulse at pin 5.

In accordance with the convention for the M system, field one line 1 number 1 starts at the first equalizing pulse, the reset of the divider system is at the start of line 4 for the first field and in the middle of line 265 for the second field.

Divider system

MODE A: LARGE (SEARCH) WINDOW

Divider ratio between 488 and 576.

This mode is valid for the following five conditions:

1. Divider is locking to a new transmitter.
2. Divider ratio found, not being within the narrow window limits.
3. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
4. External forced setting. This can be achieved by loading pin 18 with a 220 Ω resistor to earth or by connecting a 3.6 V stabistor diode between pin 18 and ground.
5. A vertical sync pulse was detected within the interval provided by reset divider (at 528) and the end of the vertical blanking while the voltage at pin 18 is ≤1.2 V.

MODE B: NARROW WINDOW

Divider ratio between 522 and 528.

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses in the large window mode. When count 12 is reached the vertical sync pulse is tested for the standard TV-norm being the divider ratio 525. When this value is valid for the 12th vertical pulse, the up/down counter is reset to 0 and the up/down counter tests for a valid 525 divider ratio. When at the 12th vertical pulse the divider ratio is not equal to n = 525 then the divider system remains in the narrow window mode and remains testing for the standard TV-norm. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

MODE C: STANDARD TV-NORM

Divider ratio 525; f_V = 60 Hz.

When the up/down counter has reached its maximum value of 12 in the narrow window mode and the divider ratio equals n = 525 the information applied to the up/down counter is changed such that now the standard divider ratio value is tested and the up/down counter is reset to 0. When the up/down counter reaches the value of 14 approved M TV-norm pulses the divider system is changed over to the standard divider ratio mode.
In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition provides maximum protection for video recorders playing tapes with anti-copy guards.

MODE D: NO TV TRANSMITTER FOUND

At pin 18 the voltage level is less than 1.2 V.

In this condition, only noise is present and no vertical sync pulse is detected, the divider is reset to count 528. In this way a stable picture display at normal height is achieved.

MODE E: VIDEO TAPE RECORDERS IN FEATURE MODE

NTSC (M system) 3-speed video tape recorders

It should be noted that some VTRs operating in the picture search mode, generate such distorted pictures that the no TV transmitter detection circuit can be activated as the voltage on pin 18 drops below 1.2 V. This would imply a rolling picture (Mode D). In general VTRs do use a re-inserted vertical pulse in the feature mode. Therefore the divider system has been designed such that the divider is forced to the wide window mode when V_{18} is below 1.2 V and a vertical sync pulse is detected within the window provided by the reset divider at 528 and the end of the vertical blanking period.

General

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the divider mode A the start is generated at the reset of the divider. In modes B and C the anti-top-flutter pulse starts at the beginning of the first equalizing pulse sequence. The anti-top-flutter ends after the second equalizing pulse sequence.

The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34, the middle of line 21 of field 1 and at the end of line 283 of field 2.

The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the B or C mode.

Vertical sawtooth

To generate a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF. The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is also activated at reset. When the capacitor has reached a voltage value of 5.0 V the voltage is kept constant until the charging period ends. The charging period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source the value of which can be set by an external resistor connected between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal Zener diode reference voltage which has a typical voltage of 7.5 V. The recommended operating current range is 10 to 75 µA. The resistor at pin 4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction voltage can be set to the required value by external components connected between pins 3 and 4 or by superimposing a correction voltage in series with the earth connection of the resistor connected to pin 4.
The vertical amplitude is set by the current of pin 4.

Vertical feedback

The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V (p-p).
The low DC voltage value improves the picture bounce behaviour as less parabola compensation is required. Even a DC-coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous voltage level of 2.5 V in the sandcastle output signal of pin 17. This results in blanking of the picture displayed, thus preventing a burnt-in horizontal line.

Vertical driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 170 Ω. The output pin is also connected to an internal current source with a sink current of 0.25 mA.

Integration time of the vertical synchronization pulse separator

The vertical sync separator has two integration times:

- long time; typical 19 µs, valid for $1.8 \leq V_{18} \leq 7.8$ V (no noise detected)
- short time; typical 12 µs, valid for noise detected and $V_{18} \geq 1.2$ V.

When V_{18} drops below 1.2 V, the integration time is forced back to 19 µs to prevent switching of the divider system to the wide window mode for noise only conditions.

Sync separator, phase detector and TV-station identification (pins 5, 6, 7 and 18)

SYNC SEPARATOR

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor connected between pins 6 and 7. The value is given by the formula:

$$p = \frac{R_S}{5.3 \times R_S} \times 100\ (R_S \text{ value in k}\Omega)\ .$$

Where R_S is the resistor connected between pins 6 and 7 and the top sync levels equals 100%. The recommended resistor value is 5.6 kΩ.

BLACK LEVEL DETECTOR

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the vertical blanking interval the slicing detector is inhibited by a signal which starts with the anti-top-flutter pulse and ends with the reset of the vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.
An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V.

NOISE LEVEL DETECTOR

The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level (S/N) of ≤19 dB is detected a counter circuit is activated.

$$S/N = 20 \log \frac{\text{Video voltage (black-to-white signal)}}{\text{Noise (RMS)}}$$

A video input signal is processed as "acceptable noise free" when 12 out of 15 sync pulses have a noise level below 19 dB for successive field periods. The sync pulses are processed during a 15 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB. The use of a filter of 1 kΩ and 150 pF in front of pin 5 reduces the noise content of the CVBS signal by approximately 6 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse detection. At the same time the integration time of the vertical sync pulse separator is reduced providing $V_{18} > 1.2$ V.

PHASE DETECTOR (SEE FIG.3)

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by a factor of 1.4.
In this way there is no requirement for external VTR time constant switching, and thus all station numbers are suitable for signals from VTR, video games or home computers.

For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a field period counter which switches the phase detector to fast for 3 field periods during the vertical scan period.
The horizontal oscillator will now lock to the new TV station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched off and the divider is set to the large window. In general the mute signal is switched off within 5 ms (C_{18} = 47 nF) after reception of a new TV signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the field counter is switched off and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to approximately 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition.
The phase detector output current during the blanking period is now reduced from 2 mA to 1.35 mA.
When desired, most conditions of the phase detector can also be set by external means in the following way:

- fast time constant, TV transmitter identification circuit not active, connect pin 18 to ground (pin 9)
- fast time constant, TV transmitter identification circuit active, connect a 220 kΩ resistor between pin 18 and ground; this condition can also be set by using a 3.6 V stabistor diode instead of a resistor
- slow time constant (with the exception of the vertical blanking period), connect pin 18 via a 10 kΩ resistor to +12 V (pin 10); in this condition the transmitter identification circuit is not active
- no switching to slow time constant required (transmitter identification circuit active), connect a 6.8 V Zener diode between pin 18 and ground.

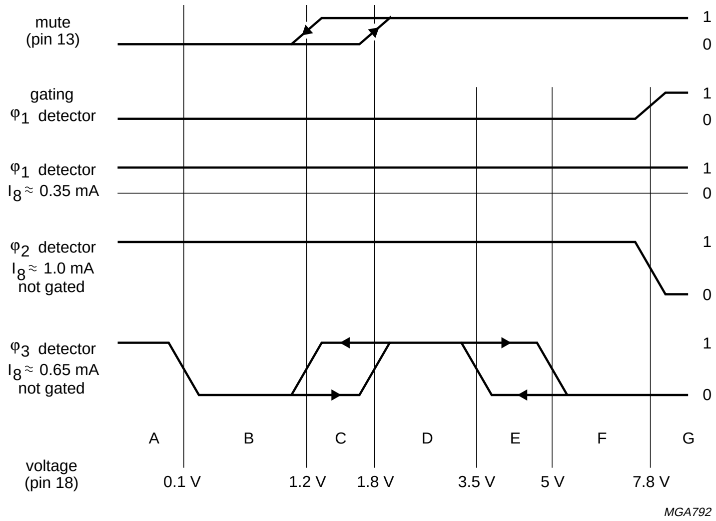


Fig.3 Operation of the three phase detector circuits.

Explanation of areas A to G shown in Fig.3

A	switching over to new TV station activates 3 field period counter
B	noise only condition
C	TV transmitter identification hysteresis range
D	fast time constant
C-E	fast time constant hysteresis range
F	normal time constant
G	sync pulse noise level detection circuit forces pin 18 to >7.8 V while signal-to-noise level <19 dB; slow time constant and gated sync pulse operation.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage operate a very low supply current into pin 16. The horizontal oscillator starts at a supply current of approximately 4 mA (V_{16} approximately 6 V). The horizontal output stage is forced into the non-conducting stage until the supply current has reached a typical value of 5 mA.

The circuit has been designed such that after starting the horizontal output function, a current drop of approximately 1 mA is allowed.

The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as oscillator signal for synchronized switched-mode power supplies.

The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C).
The main supply should be connected to pin 10 and pin 9 should be used for ground. When the voltage on pin 10 increases from zero to its final value (typ. 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes and the voltage on pin 16 will stabilize on a typical value of 9.3 V. In stabilized conditions (V_{10} > 10 V) the minimum required supply current into pin 16 is approximately 2.5 mA.
All other IC functions are switched on via the main supply voltage on pin 10. When this voltage reaches a value of approximately 7 V the horizontal phase detector is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 typical 9.3 V.

To close the second phase detector loop a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.
For remote switch-off pin 16 can be connected to ground (via a npn transistor with a collector series resistor of approximately 500 Ω) which decreases pin 16 voltage to ≤5 V and switches off the horizontal output pulse.

Horizontal oscillator, horizontal output transistor and second phase detector

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground (pin 9). The open collector horizontal output stage is connected to pin 11. An internal Zener diode configuration limits the open voltage of pin 11 to approximately 14.5 V. The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of approximately 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of approximately 40% HIGH.
The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched off and the second phase detector is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%. The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output state.

The horizontal output pulse duration is 29 µs HIGH for storage times between 1 µs and 17 µs (flyback pulse of 12 to 29 µs). A higher storage time increases the HIGH time.
Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV transmitter) the npn transistor is switched on. When the voltage on pin 18 increases to a level of approximately 1.8 V (new TV transmitter found) the npn transistor is switched off.
This function is available when pin 13 is connected to pin 10 (+12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV transmitter is identified the voltage on pin 13 will be LOW (<0.5 V).
When an M-system TV transmitter with a divider ratio <576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force the output voltage down to approximately 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17 has three different voltage levels. The highest level (10.4 V) can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12 and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 60 Hz the blanking pulse duration is 34 clock pulses started from the reset of the vertical divider system.

For TV signals which have a divider ratio between 522 and 528 the vertical blanking pulse is started at the first equalizing pulse.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{16}	start current	V_{10} = 0 V	–	9.7	mA
V_P	supply voltage		–	13.2	V
P_{tot}	total power dissipation		–	1.2	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	50 K/W

CHARACTERISTICS

$V_P = V_{10}$ = 12 V; I_{16} = 6.2 mA; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 10)		10	12	13.2	V
I_{16}	supply current (pin 16)	note 1				
		V_{10} = 0 V	6.2	–	9.7	mA
		V_{10} = 1 to 10 V; $T_{amb} \leq 70$ °C	6.2	–	8.7	mA
		V_{10} > 10 V	2.5	–	9.7	mA
V_{16}	stabilized voltage (pin 16)		8.8	9.3	9.7	V
I_{10}	current consumption (pin 10)		–	70	85	mA
Video input (pin 5)						
V_5	top sync level		1.5	3.1	3.75	V
$V_{5(p\text{-}p)}$	sync pulse amplitude (peak-to-peak value)	note 2	0.05	0.6	1	V
SL	slicing level	note 3	35	50	65	%
t_d	delay between video input and detector output	see Fig.5	0.2	0.3	0.55	µs
S/N	signal-to-noise ratio with sync pulse noise level detector circuit active	CVBS = 1 V without filter at pin 5; note 4	–	19	–	dB
Sync pulse						
HYS	noise level detector circuit hysteresis		–	3	–	dB
Noise gate (pin 5)						
V_5	switching level		–	0.7	1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
First control loop (pin 8) horizontal oscillator to synchronization signal						
Δf	holding range		±700	±800	–	Hz
Δf	catching range		±700	±800	±1100	Hz
α_{CS}	control sensitivity video with respect to burst key and flyback pulse:					
	slow time constant	note 5	–	2	–	kHz/µs
	normal time constant	note 6	–	5	–	kHz/µs
	fast time constant	note 6	–	3	–	kHz/µs
φ_{10}	phase modulation due to hum on the supply line (peak-to-peak value)	note 7	–	0.2	–	µs/V
φ_{16}	phase modulation due to hum on the input current (peak-to-peak value)	note 8	–	0.08	–	µs/V
Second control loop (pin 14) horizontal flyback to horizontal oscillator						
$\Delta t_d/\Delta t_o$	control sensitivity	t_d = 10 µs	200	300	600	µs/µs
t_d	control range		1	–	45	µs
t_d	control range for constant duty factor horizontal output		1	29 – t_{FB}	–	µs
	control edge of horizontal output signal (pin 11)		–	positive	–	
Phase adjustment (pin 14) via second control loop						
α_{CS}	control sensitivity	t_d = 10 µs	–	25	–	µA/µs
I_{14}	maximum allowed control current		–	–	±60	µA
Horizontal oscillator (pin 15) C_{osc} = 2.7 nF; R_{osc} = 34.2 kΩ						
f_H	frequency (no sync)		–	15 625	–	Hz
Δf_H	spread (fixed external components, no sync)		–	–	±4	%
Δf_H	frequency deviation between starting point output signal and stabilized condition		–	+5	+8	%
TC	temperature coefficient		–	-1.10^{-4}	–	K
Horizontal output (pin 11) open collector						
V_{11H}	HIGH level output voltage		–	–	13.2	V
V_{11}	start voltage protection (internal Zener diode)		13	–	15.8	V
I_{16L}	LOW level input current protection output enabled		–	5.0	6.2	mA
V_{11L}	LOW level output voltage start condition	I_{11} = 10 mA	–	0.1	0.5	V
δ	duty factor output current during starting	I_{16} = 6.2 mA	50	60	70	%
V_{11L}	LOW level output voltage normal condition	I_{11} = 25 mA	–	0.3	0.5	V
δ	duty factor output current without flyback pulse pin 12		45	50	55	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{OH}	duration of output pulse HIGH	storage time horizontal deflection stage = 10 μs	27	29	31	μs
TC	temperature coefficient		–	-4.10^{-2}	–	K
$\Delta H_W/H_d$	influence of delay time on pulse width of horizontal output signal		–	0.16	–	μs/μs
	controlled edge		–	positive	–	
Sandcastle output signal (pin 17)						
V_{17}	output voltage during:					
	burst key		9.8	10.4	–	V
	horizontal blanking	I_{load} = 1 mA	4.1	4.5	4.9	V
	vertical blanking	I_{load} = 0.3 mA	2.1	2.5	2.9	V
V_{17}	zero level output voltage	I_{sink} = 0.5 mA	–	0.7	–	V
t_P	burst key pulse width	60 Hz	3.4	3.65	4	μs
V_{12}	horizontal blanking level		–	1	–	V
	vertical blanking	note 9				
t_{d1}	phase position burst key time between middle sync pulse at pin 5 and start burst key pulse at pin 17		2.3	2.7	3.1	μs
t_{d2}	phase position burst key time between start sync pulse at pin 5 and end of burst key pulse at pin 17	60 Hz	–	–	9.1	μs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see Fig.1)						
I_{18}	detector output current		–	0.25	–	mA
V_{18}	voltage level for in sync condition	φ_1 normal	5.8	6.4	7	V
V_{18}	voltage level for noisy sync pulse	φ_1 slow and gated	9	10.1	–	V
V_{18}	voltage level for noise only	note 10	–	0.3	–	V
V_{18}	switching level:					
	normal to fast		<3.2	3.5	3.8	V
	mute output active and fast to normal		<1.0	1.2	1.4	V
	field period counter	3 periods fast	<0.08	0.12	0.16	V
	normal to fast mute output inactive	locking	>1.5	1.75	2	V
	fast to normal	locking	>4.7	5	5.3	V
	normal to slow	gated sync pulse	>7.4	7.8	8.2	V
Video transmitter identification output (pin 13)						
V_{13}	output voltage active	no sync; I_{13} = 2 mA	–	0.15	0.32	V
I_{13}	sink current active	no sync; V_{13} = 1 V	–	–	5	mA
I_{13}	output current inactive	sync 60 Hz	–	–	1	μA
60 Hz identification (pin 13) R_{13} positive supply 15 kΩ						
V_{13}	pnp emitter follower voltage	note 11	7.2	7.65	8.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input pulse (pin 12)						
V_{12}	switching voltage level		–	0.9	–	V
I_{12}	input current		0.2	–	3	mA
$V_{12(p-p)}$	input pulse (peak-to-peak value)		–	–	12	V
R_{12}	input resistance		–	3.5	–	kΩ
t_d	phase position without shift; time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		2.1	2.5	2.9	μs
Vertical ramp generator (pin 3)						
t_c	charge current pulse width		–	$26t_{clk}$	–	
I_3	charge current		–	3	–	mA
V_3	top level ramp signal voltage divider in 60 Hz mode	note 12	4.55	4.85	5.25	V
$V_{3(p-p)}$	ramp amplitude (peak-to-peak value); R_4 = 330 kΩ; f_V = 60 Hz	C_3 = 150 nF; note 12	–	2.5	–	V
Current source (pin 4)						
V_4	output voltage	I_4 = 20 μA	7	7.5	7.9	V
I_4	allowed current range	T_{amb} = 25 to 70 °C	10	–	75	μA
TC	temperature coefficient output voltage	I_4 = 40 μA	–	50	–	10^{-6}/K
Current source (pin 3)						
$I_{3/4}$	current ratio pin 3/pin 4	I_4 = 35 μA; V_3 = 2 V	–	1.05	–	
TC	temperature coefficient I_3	I_4 = 40 μA; R_4 fixed	–	100	–	10^{-6}/K
Comparator (pin 2)						
V_2	input voltage DC level	R_4 = 330 kΩ; C_3 = 150 nF	0.98	1.075	1.17	V
$V_{2(p-p)}$	input voltage AC level (peak-to-peak value)	R_4 = 330 kΩ; C_3 = 150 nF	–	0.8	–	V
I_2	input current	V_2 = 0 V	–	–	1	μA
Vertical output stage (pin 1) npn emitter follower						
V_1	maximum output voltage	I_1 = +1.5 mA; note 12	5	5.5	6.3	V
R_S	sync separator resistor		–	170	–	Ω
I_{sink}	continuous sink current		–	0.25	–	mA
Vertical guard circuit (pin 2)						
V_{2H}	active switching level HIGH	V_{17} = 2.5 V; note 12	>1.7	1.85	2.0	V
V_{2L}	active switching level LOW	V_{17} = 2.5 V; note 12	<0.25	0.35	0.45	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal vertical sync pulse separator						
t_{d1}	delay between video signal at pin 5 and internally separated vertical sync pulse; normal signal condition		12	19	25	μs
t_{d2}	delay between video signal at pin 5 and internally separated vertical sync pulse; noisy signal condition	$V_{18} \geq 1.2$ V	–	–	–17	μs

Notes to the characteristics

1. Value inclusive R_L pin 11 to pin 16 = 6.8 kΩ.
2. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is fixed by the formula:

   $$p = \frac{R_s}{5.3 \times R_s} \times 100\%.$$

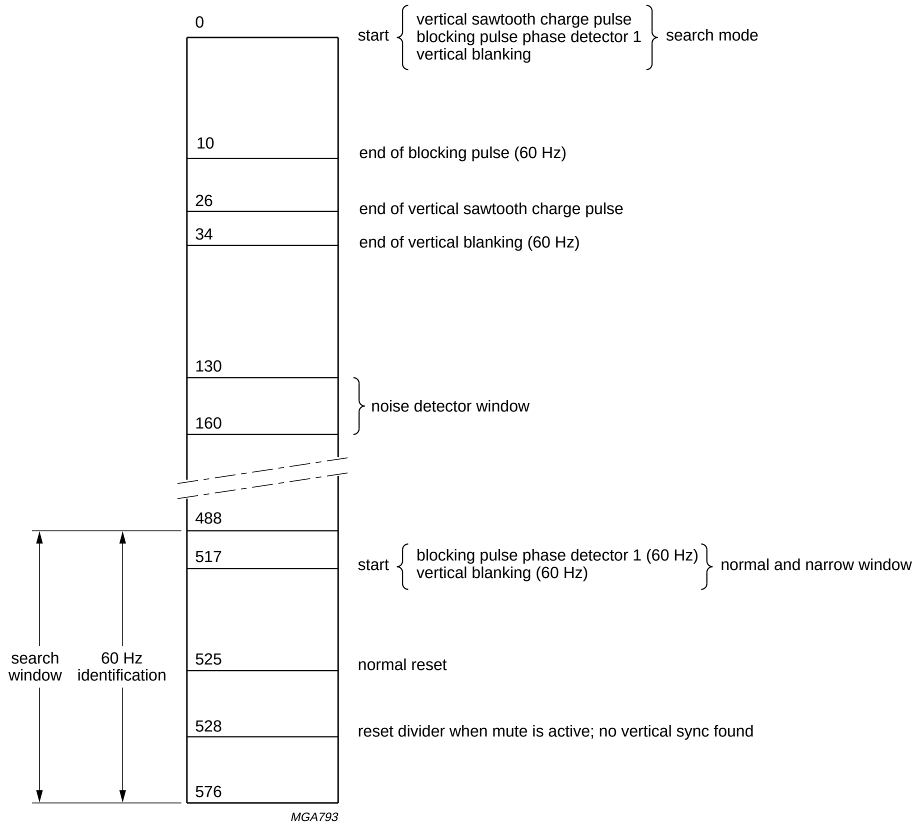
   Where R_S is the resistor between pins 6 and in kΩ; top sync = 100%.
4. $$S/N = 20 \log \frac{\text{Video voltage (black-to-white signal)}}{\text{Noise (RMS)}}$$

   A low-pass filter of 1 kΩ and 150 pF decreases the noise content of the CVBS signal by 6 dB.
5. Undercompensated.
6. Overcompensated.
7. Measured between pin 5 and sandcastle output pin 17.
8. Measured with 3.3 μF feedback capacitor between pin 16 and 6.8 μF capacitor in PLL filter pin 8.
9. Maximum divider ratio (60 Hz):

   $$n = \frac{2 \times f_H}{f_V} = 576 \text{ (2 clock pulses per video line).}$$

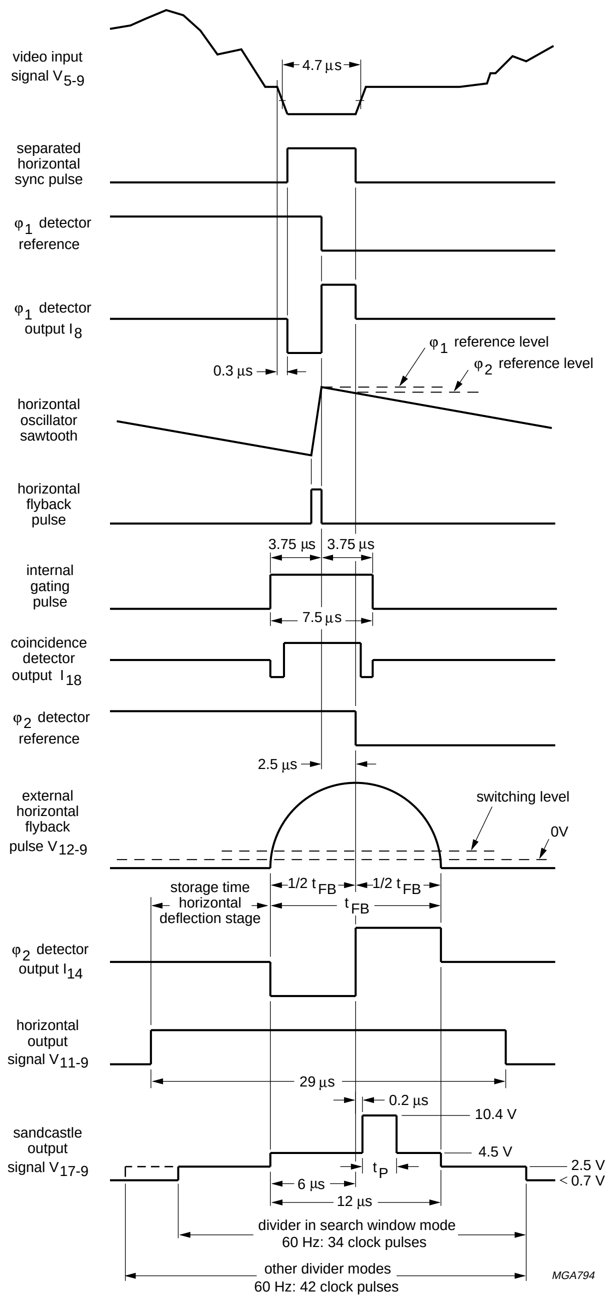
   Start vertical blanking:
   - search (large) window mode (60 Hz)
   - reset divider = start vertical sync pulse plus 1 clock pulse
   - small/standard window mode (60 Hz)
   - clock pulse 517.

   Stop vertical blanking:
   - all window modes (60 Hz)
   - clock pulse 34.
10. Depends on DC level of pin 5, value given is valid for $V_5 \approx 5$ V.
11. Valid for $\frac{2 \times f_H}{f_V} < 576$.
12. Value related to internal Zener diode reference voltage. Spread includes complete spread of reference voltage.



One video line equals two counter pulses.
Reset counter 32 µs after start of vertical sync pulse at pin 5.
Reset counter = counter state 0.

Fig.4 Counter system.



Two counter pulses equals one video line.

Fig.5 Timing diagram.

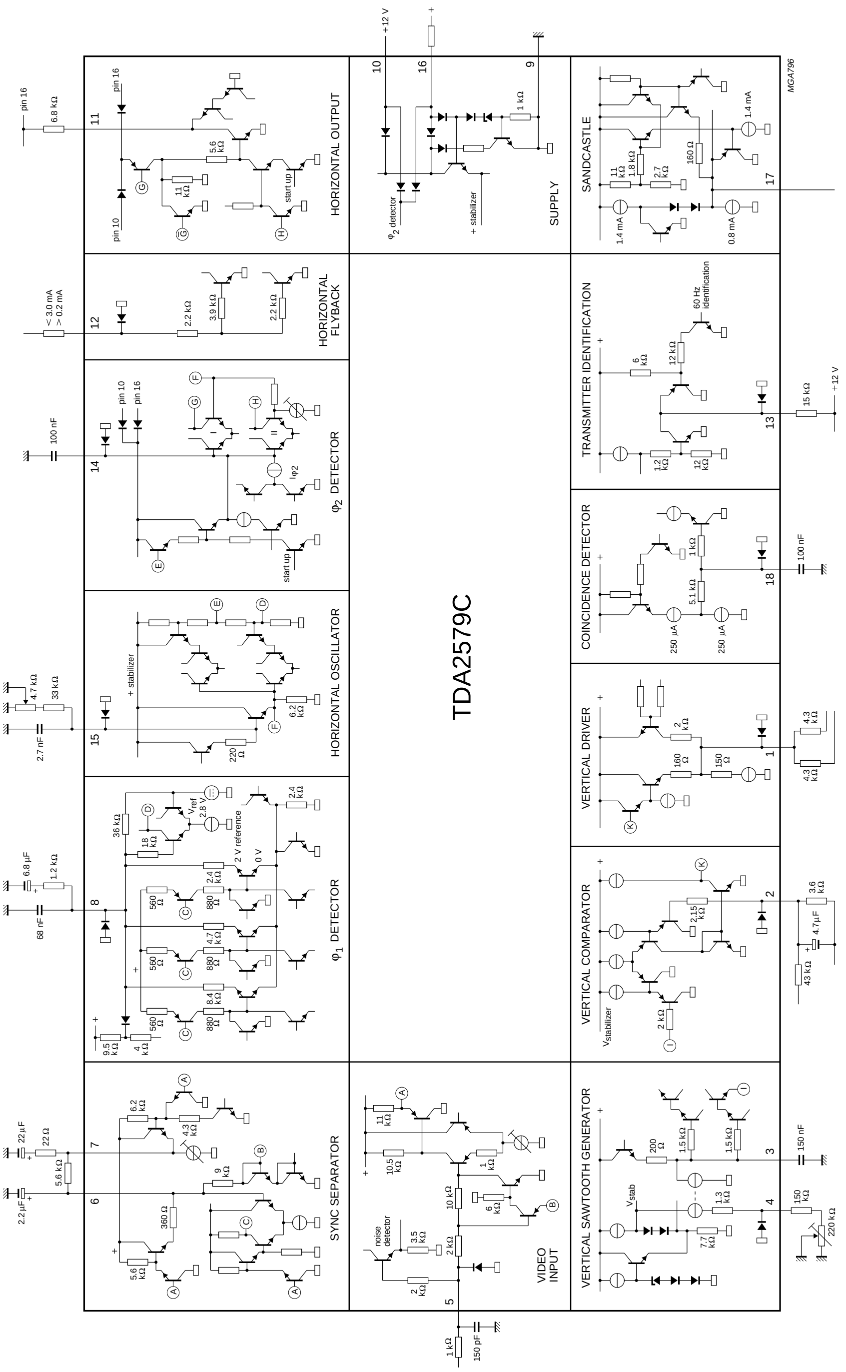
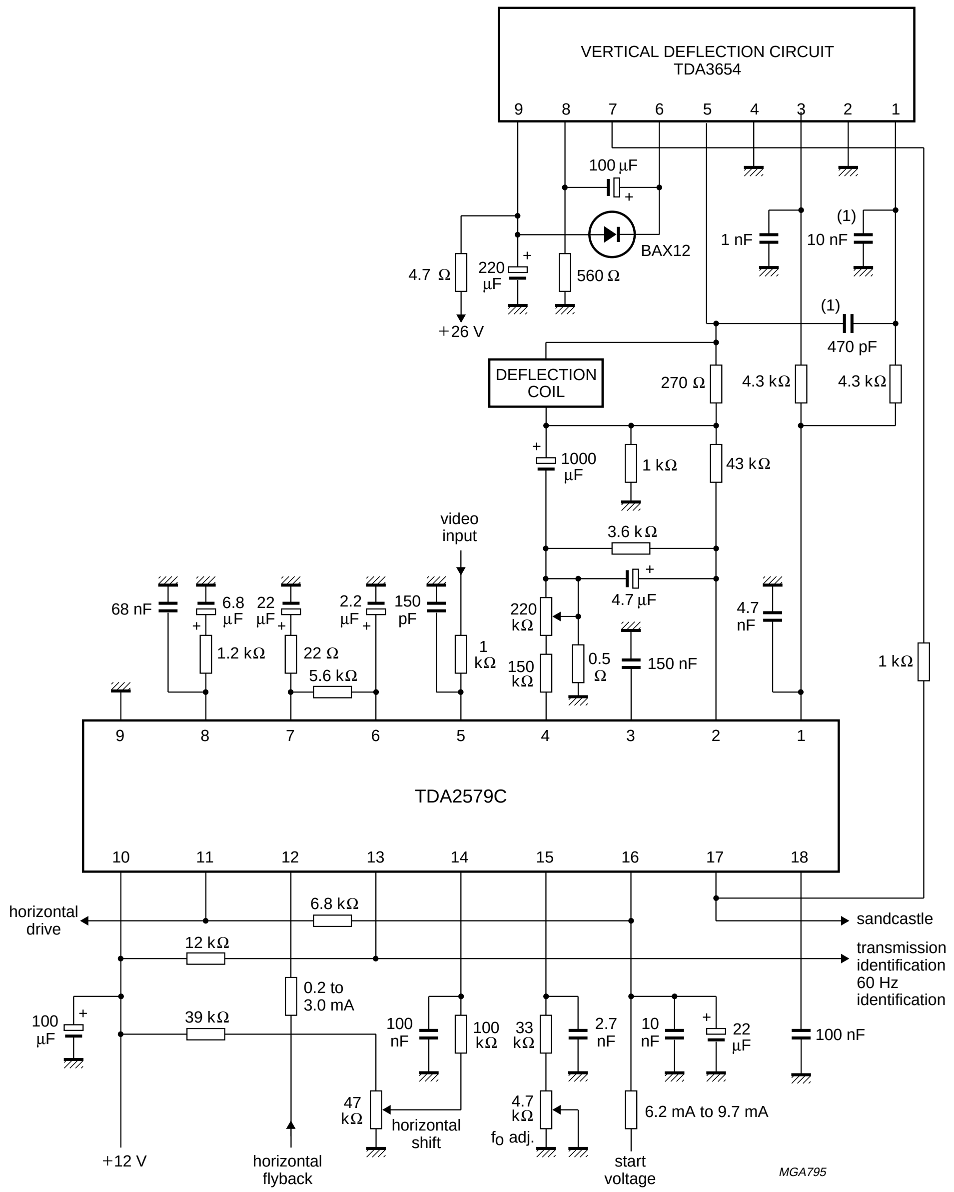


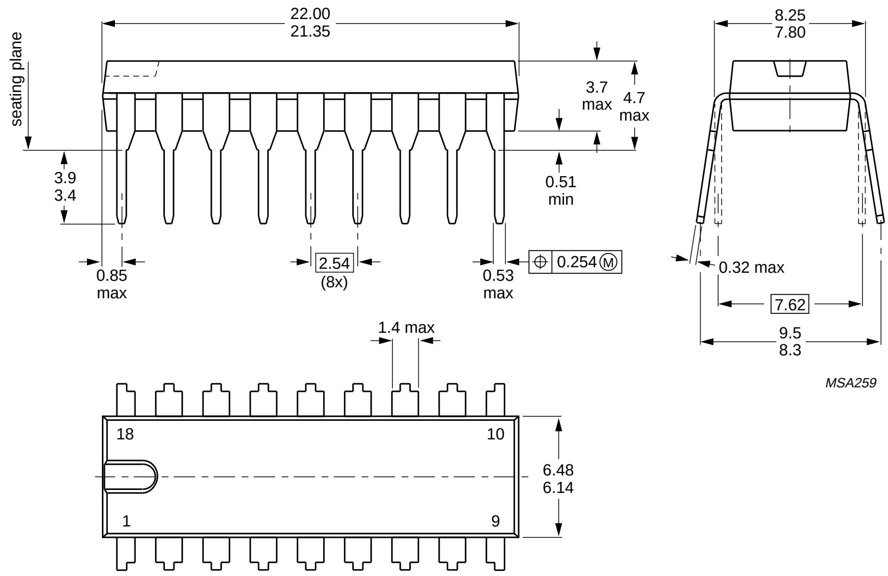
Fig.6 Internal circuitry



(1) Dependent on printed-circuit board layout.

Fig.7 TDA2579C and TDA3654 combination 110° Flat Square picture tube.

PACKAGE OUTLINE



Dimensions in mm.

Fig.8 18-lead dual in-line; plastic (SOT102).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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